FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
2210.0020002	10/040,852
FIRST NAMED INVENTOR: Tommy K. Eng	
FILING DATE: December 28, 2001	ART UNIT: 2825

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
TD	AA1	6,360,356 B1	March 19, 2002	Eng			
	AB1						
	AC1						
	AD1						
	AE1						
	AF1						
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

TD	AR	1	Alcatel Telecommunications Review, 2nd Quarter, 1996, The Challenge of Designing Million-Transistor ASICs, H. Casier et al., pages 122-129
TD	AS	1	31st Design Automation Conference®, San Diego, CA, June 6-10, 1994, Technology Mapping Using Fuzzy Logic, Sasan Iman et al., pages 333-338
TD	AT	1	Layout Driven Technology Mapping, Massoud Pedram et al., 28th ACM/IEEE Design Automation Conference, pages 99-105

EXAMINER	DATE CONSIDERED
Mwando	11-15-04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2						
	AB2						
	AC2						
	AD2						
	AE2						
	AF2						
	AG2						
	AH2						
	AI2						
	AJ2						
	AK2						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

TD	AR	2	Hewlett-Packard Journal, February 1995, Volume 46, Number 1, Shortening the Time to Volume Production of High-Performance Standard Cell ASICs, Jay D. McDougal et al., pages 91-96
TD	AS	2	Layout-Driven RTL Binding Techniques for High-Level Syntrhesis, Min Xu et al., 1996 IEEE, pages 33-38
TD	AT	2	Proceedings of the IEEE 1989 Custom Integrated Circuits Conference, May 15-18, 1989, LOGOPT- A Multi-Level Logic Synthesis and Optimization System, Ajit M. Prabhu, pages 4.1.1 - 4.1.4

EXAMINER: Nguyen DATE CONSIDERED: 11-15-04

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